

WHAT IS CLAIMED IS:

1 1. A SYNC pulse compensation apparatus, comprising:
2 a sampling compensation circuit operable to
3 condition a SYNC pulse signal, wherein said SYNC pulse signal
4 is based on a predetermined temporal relationship between a
5 first clock signal operable to clock a first circuit portion
6 and a second clock signal operable to clock a second circuit
7 portion; and

8 a jitter cycle delay compensation circuit coupled
9 to said sampling compensation circuit, said jitter cycle
10 delay compensation circuit operating to tap said SYNC pulse
11 signal after a predetermined delay based on a skew difference
12 between said first and second clock signals.

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1 2. The SYNC pulse compensation apparatus as set forth
2 in claim 1, wherein said sampling compensation circuit
3 comprises a plurality of multiplexers arranged in series,
4 each multiplexer operating to receive an input through a
5 timing register associated therewith.

1 3. The SYNC pulse compensation apparatus as set forth
2 in claim 2, wherein said multiplexers are operable to insert
3 a logic high condition in said SYNC pulse signal when said
4 SYNC pulse signal is sampled to contain a plurality of logic
5 lows during a predetermined time window.

1 4. The SYNC pulse compensation apparatus as set forth
2 in claim 2, wherein said plurality of multiplexers comprises
3 three multiplexers operable to insert a [010] sequence in
4 said SYNC pulse signal when said SYNC pulse signal is sampled
5 to be all zeros during a predetermined time window.

1 5. The SYNC pulse compensation apparatus as set forth
2 in claim 1, wherein said jitter cycle delay compensation
3 circuit comprises:

4 a series of delay registers, each operating to
5 delay said SYNC pulse signal by a predetermined amount of
6 time; and

7 a multiplexer operable to select a delayed SYNC
8 pulse output generated from said series of delay registers.

1 6. The SYNC pulse compensation apparatus as set forth
2 in claim 5, wherein said series of delay registers comprises
3 eight registers.

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1 7. The SYNC pulse compensation apparatus as set forth
2 in claim 5, wherein said multiplexer is actuated by a JITTER-
3 STATE control signal generated by a state/correct block
4 responsive to said skew difference between said first and
5 second clock signals.

1 8. The SYNC pulse compensation apparatus as set forth
2 in claim 7, wherein said state/correct block is coupled to
3 a phase detector operating to detect said skew difference
4 between said first and second clock signals.

1 9. The SYNC pulse compensation apparatus as set forth
2 in claim 7, wherein said JITTER-STATE control signal is
3 stored in a flip-flop.

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1 10. A SYNC pulse compensation method, comprising the
2 steps:

3 sampling a SYNC pulse signal generated based on a
4 predetermined temporal relationship between a first clock
5 signal operable to clock a first circuit portion and a second
6 clock signal operable to clock a second circuit portion; and

7 if said SYNC pulse signal is sampled to contain a
8 plurality of a logic lows during a predetermined time period,
9 inserting a logic high condition at a select point in time.

1 11. The SYNC pulse compensation method as set forth in
2 claim 10, wherein said second clock signal is generated by
3 a phase-locked loop (PLL) based on said first clock signal.

1 12. The SYNC pulse compensation method as set forth in
2 claim 10, wherein said SYNC pulse signal is generated when
3 a rising edge in said first clock signal coincides with a
4 rising edge in said second clock signal.

1 13. The SYNC pulse compensation method as set forth in
2 claim 12, further comprising the step:

3 if said SYNC pulse signal is sampled to indicate
4 a duplicate logic high condition during a predetermined time
5 period, masking said duplicate logic high condition.

1 14. A SYNC pulse compensation method, comprising the
2 steps:

3 sampling a SYNC pulse signal generated based on a
4 predetermined temporal relationship between a first clock
5 signal operable to clock a first circuit portion and a second
6 clock signal operable to clock a second circuit portion;

7 determining a clock state indicative of a phase
8 difference between said first and second clock signals;

9 re-positioning said SYNC pulse signal based on said
10 clock state; and

11 if said SYNC pulse signal is out-of-phase by a
12 predetermined amount with respect to said first clock signal,
13 delaying said SYNC pulse signal based on said clock state.

1 15. The SYNC pulse compensation method as set forth in
2 claim 14, wherein said SYNC pulse signal is re-positioned by
3 adding at least an extra clock cycle when said clock state
4 indicates that said first clock signal lags with respect to
5 said second clock signal by a predetermined amount.

6 16. The SYNC pulse compensation method as set forth in
7 claim 14, wherein said SYNC pulse signal is re-positioned by
8 deleting at least an extra clock cycle when said clock state
9 indicates that said second clock signal lags with respect to
said first clock signal by a predetermined amount.

1 17. The SYNC pulse compensation method as set forth in
2 claim 14, wherein said SYNC pulse signal is delayed by
3 propagating said SYNC pulse signal through a series of delay
4 registers operable to be selected by a multiplexer in
5 response to a JITTER-STATE control signal corresponding to
6 said clock state.

1 18. The SYNC pulse compensation method as set forth in
2 claim 17, wherein said JITTER-STATE control signal is stored
3 in at least one flip-flop.

1 19. The SYNC pulse compensation method as set forth in
2 claim 14, wherein said first and second clock signals
3 comprise a core clock and a bus clock, respectively, in a
4 computer system.